



HELGEN EINARBOARD 1.0

HBOX RTK Watchdog Carrier — Production Engineering Manual

Rev 1.1 — Post-Audit Production Master

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Project	Drogheda (GPS RTK) — Hutchison Ports ICAVE / TIMSA / EIT / LCT
KiCad project	kicad/hbox-watchdog-v3-PROD.kicad_pcb
Board	135.1 × 100.1 mm, 4-layer, 132 footprints, 130 nets
Verification	ERC 0 errors · DRC 0 errors / 0 unconnected (2026-07-07)
Author	Helgen CTO/CSO — principal HW/SW architect
Status	Bare-board order RELEASED · PCBA gated (§10)

Revision history

Rev	Date	Change
1.0	2026-07-06	Initial production master; pre-fab audit executed same day (4 HIGH, 6 MED findings).
1.1	2026-07-07	Post-audit master. H1 Q7 S/D corrected (S=VIN_SW, D=MAIN5V); H2 Q5/Q6 to Q_NPN_BEC map; H3 RIG1/RDFU1=22 k Ω + dangling pin fixed; H4 SW_IN in PWR_MID @1.0 mm. M3 closed (physical Pro pinout verified). Refdes converged to numbered names. Fab package regenerated after last save.

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1 System overview

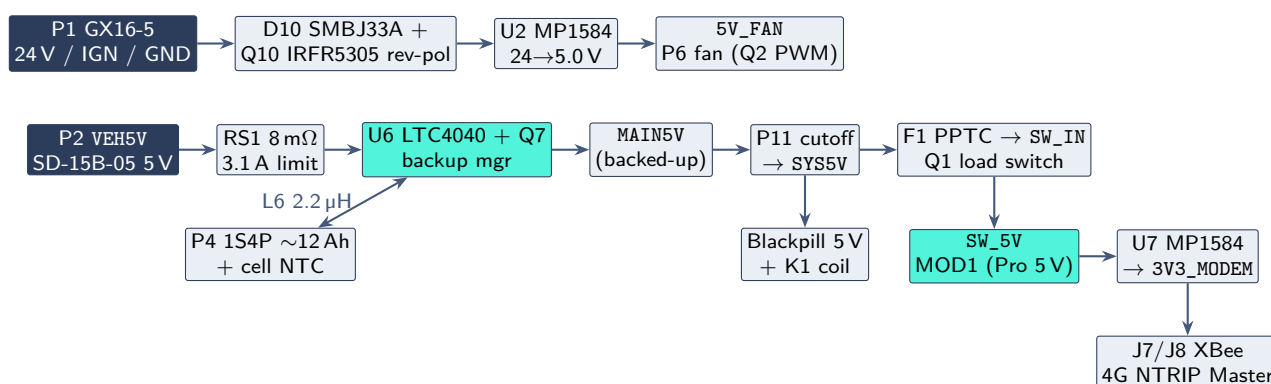
EinarBoard 1.0 (title-block *EINARBoard HBOX 1.0*; KiCad lineage `hbox-watchdog-v3-PROD`) is the HBOX carrier/motherboard for the Drogheda GPS-RTK fleet tracker deployed on heavy port equipment. It hosts the full electronics stack of an HBOX unit on plug-in sockets and carries the watchdog, power, backup-battery, thermal-sensing, and fail-safe corrections infrastructure on its own copper:

- **STM32F411 Blackpill** (watchdog MCU) on J1/J2 1×20 sockets — supervises the stack, power-cycles it on lost corrections, gauges the battery, qualifies charging by temperature, and injects \$PHLG diagnostics on the Modo-B uplink.

- **simpleRTK2B Pro** (u-blox ZED-F9P) as an Arduino-UNO-form shield on MOD1 — GNSS RTK engine.
- **4G NTRIP Master** (XBee-form LTE) on J7/J8 2.00 mm sockets at 3V3_MODEM — corrections downlink and NMEA uplink. USB-C service port J9 firmware-updates the modem in place.
- **LTC4040** battery-backup manager with a 1S4P (~12 Ah) 18650 pack — rides through power loss on a parked machine; charge voltage strapped to 4.00 V Li-ion for cycle life and hot-cell margin (RCA #1 answer).
- **K1 normally-closed relay bypass** — RTCM3 corrections survive a dead, hung, or physically absent MCU.

Deployment context: machine power (12/24 V classes at ICARE) enters the IP67 cabinet (breaker, SPD, Mean Well DDR-60G-24); the HBOX receives regulated 24 V, vehicle 5 V (SD-15B-05), and *raw* machine ignition through the GX16-5 bulkhead. Corrections arrive over LTE/NTRIP — never through the GNSS — so link recovery is always a stack power-cycle.

1.1 Power tree (as built, Rev 1.1)



Ignition sense (Rev 1.1 topology — DFR1015 removed): GX16 pin 3 carries *raw* machine ignition (12–24 V) to IGN_IN → RIG1 22 kΩ / RIGb 10 kΩ divider → D5 BAT54 clamp to 3V3 + C9 100 nF → PA5 (digital input). At 24 V the clamp carries <1 mA. *The stale 100 Ω value (audit H3) would have burned D5 and the resistor at 24 V — corrected on board, schematic, and fab BOM.*

2 Canonical invariants (engineering memory)

Every change to this board is checked against the project ethos. In copper, Rev 1.1 realizes them as:

1. **Power-off is the safe state.** R2 10 kΩ pulls the Q1 gate to rail; only PA1 (PWR_CTRL) via Q5 can enable the RTK stack. MCU absent ⇒ stack OFF.
2. **Never vanish, never loop.** Watchdog power-cycles the stack (modem included, via U7 fed from SW_5V) instead of letting a unit go silent; firmware rate-limits reboots.
3. **Corrections ride the 4G modem, not the GNSS.** RTCM3 downlink (modem DOUT → MOD1 D2 → F9P RX2) is hardwired and never touches the MCU; uplink survives a dead MCU through K1's NC contacts.
4. **No sub-80 °C-softening material in the thermal path;** enclosure is ASA; cooling is conduction (IP67 — no vents). Thermal telemetry: SHT40 + TMP102 (I²C) + hotspot NTC (PB1) + cell NTC (charger-owned).
5. **Backend must not black-hole a healthy unit** — board-side contribution is honest telemetry (\$PHLG, charge status, temperatures) on the STREAM log.
6. **No secrets in the repo** — this manual and the BOM workbook carry none.

3 Electrical architecture by block

Block	Function	Key parts / nets
A	Fan buck 24 V→5.0 V, dedicated rail (inrush never sags MAIN5V)	U2 MP1584EN, L2 10 μ H, FB 100k/19.1k, 5V_FAN, JP1 OPEN
B	Battery backup: charger + power path + 2.5 A boost	U6 LTC4040, Q7 AO4406A, RS1 8 m Ω , L6 2.2 μ H, P4, straps 4.00 V
C	Reset	SW1 on-board + P10 external → NRST
D	4-LED battery gauge	PB12–15, RB1–4 330 Ω , DB1–4
E	Power cutoff (kills vehicle <i>and</i> battery)	P11 in series MAIN5V→SYS5V; jumper plug when unused
F	Vehicle-power sense on the vehicle side	PA4 divider taps VEH5V (never the backed-up rail)
H	Modo-B fail-safe uplink bypass	K1 G5V-1 NC, Q6 driver (PB5), D6 flyback
I	Hot-spot NTC channel	R42 10 k Ω 1% + C24 → PB1 (ADC1_IN9), P12 probe
J	Carrier sockets	J1/J2 Blackpill · MOD1 UNO shield · J7/J8 XBee 2.00 mm
K	Modem rail	U7 MP1584EN SW_5V→3V3_MODEM (3.33 V), FB 100k/31.6k
U	USB-C service port (modem DFU in place)	J9 USB4085, Rcc 5.1 k Ω × 2, SW4G reset, D4G/Rmled LED

3.1 Block B — LTC4040 backup manager (sized to the 12 Ah pack)

Single-inductor architecture: step-down charger (VSYS→BAT) while input is good; 2.5 A step-up backup (BAT→VSYS) when PFI trips. Q7 (gate = IGATE) disconnects the dead input during backup — **Rev 1.1 orientation: S = VIN_SW, D = MAIN5V** (audit H1: reversed, the body diode would have back-fed the dead vehicle rail and collapsed backup *exactly when needed*).

Parameter	Value	Sizing (ADI 4040fb)
Charge current	2.42 A $\approx$ C/5	$I_{CHG} = 2000/R_{PROG}$, $R_{PROG} = 825 \Omega$ 1% (R50)
Input current limit	3.1 A	25 mV/ R_S , $R_S = 8 m\Omega$ (RS1) — protects the SD-15B-05 (3 A); charge sheds first
PFI trip	4.60 V falling ($\approx$ 4.72 V recover)	287k/100k from VEH5V (R51/R52)
Backup voltage	4.79 V (RST -7.5% $\approx$ 4.43 V)	BSTFB=RSTFB shared divider 499k/100k (R53/R54)
Charge voltage	4.00 V Li-ion	F2=1, F1=0, F0=1 via JP2/3/4 strapped to VSYS (chemistry survives absent MCU); LiFePO ₄ = re-strap F2
Inductor	2.2 μ H, $I_{sat} \geq 8$ A	L6 (Sunlord MWSA0804S-2R2MT sub)
VSYS hold-up	104 μ F $\geq$ 100 μ F min	C32/C33 47 μ F 1210 + C34
Cell NTC	charger-owned (U6 NTC pin)	RT1 on the cell via P4.3; R55 10 k Ω bias — charging stays temperature-qualified with the MCU dead
CHGOFF	CHRG_EN (PA8) + 100 k Ω pull-down	MCU absent $\Rightarrow$ charging enabled, NTC still guards; MCU cuts charge on hot cell (RCA #1)

Safety-timer note: a deep-discharge full recharge (12 Ah @ 2.42 A $\approx$ 5 h) exceeds the internal safety timer — firmware restarts the cycle via CHRG_EN while the cell is cool and BAT_SENSE is low.

3.2 Block H — fail-safe Modo-B bypass

K1 (Omron G5V-1, 5 V coil) de-energized routes F9P TX2 → 4G DIN through its **normally-closed** contacts: corrections and position flow exactly as if the watchdog were not there — with the Blackpill

hung, unpowered, or physically removed. PB5 (BYP_CTRL) via Q6 energizes the coil to insert the MCU in-line (USART1: PA10 monitor tap, PA9 injection of \$PHLG). Verified against the Omron datasheet at net level: coil pins 2/9, COM 5&6 (internally doubled), NC = 1 = F9P TX2, NO = 10 = PA9. Q6 is a Rev 1.1 (H2) BEC-map correction — with the old BCE map it could not sink the 30 mA coil and Modo-B injection was dead.

4 Pinout matrices

4.1 STM32F411 Blackpill core signals (J1/J2 sockets)

SWD is not on the 2×20 — flash via USB-C DFU (BOOT0), diagnose via USB CDC STREAM log.

Pin	Hdr	Net	Group	Function / notes
PA0	J1	BAT_SENSE	ADC	Pack voltage $\div 2$ (R5/R6) — feeds gauge logic
PA1	J1	PWR_CTRL	Relay/Switch	RTK-stack load-switch enable via Q5→Q1; HIGH = stack ON; pull-down default OFF (invariant #1)
PA2	J1	GNSS_TX	UART	USART2 TX → MOD1 D1 (F9P UART1 RX)
PA3	J1	GNSS_RX	UART	USART2 RX ← MOD1 D0 (F9P UART1 TX) — NMEA
PA4	J1	5V_SENSE	ADC	Vehicle 5 V present, $\div 2$ from VEH5V (vehicle side — Block F; on the backed-up rail it would never drop and the cell would drain)
PA5	J1	IGN_SENSE	Ignition	Digital INPUT_PULLDOWN; raw 12–24 V → 22k/10k divider + BAT54 clamp + 100 nF (Rev 1.1/H3)
PA6	J1	FAN_PWM	PWM	TIM3_CH1, 25 kHz → Q2 low-side
PA7	J1	—	Reserve	Proto-only LM35 channel; unassigned on EinarBoard
PA8	J2/5	CHRG_EN	LTC status	U6 CHGOFF; HIGH = charge OFF; 100 k Ω pull-down = charging enabled if MCU absent (NTC still guards). <i>Proto TP4056 rig is INVERTED (CHRG_RUN) — firmware flag</i>
PA9	J2	USART1_TX	UART/Modo-B	→ K1 NO — \$PHLG injection when K1 energized
PA10	J2/7	USART1_RX	UART/Modo-B	← F9P TX2 (K1 NC node, MOD1 D8) — passive monitor tap
PB0	J1/14	EXT_LED	GPIO	Status LED low-side (Q4); panel LED on P8
PB1	J1/15	NTC_TEMP	ADC	ADC1_IN9 hotspot NTC (R42 10 k 1% + C24; P12 probe at battery/modem) — may drive the charge cutoff
PB3	J2/11	CHRG_STAT	LTC status	U6 CHRG open-drain, 100 k $\uparrow$ 3V3; LOW = charging ($>C/8$)
PB4	J2/12	CHRG_FAULT	LTC status	U6 FAULT open-drain, 100 k $\uparrow$ 3V3; LOW = NTC/bad-battery fault
PB5	J2/13	BYP_CTRL	Relay control	K1 coil driver via Q6 (BEC map — Rev 1.1/H2); HIGH = MCU in-line on the uplink; de-energized/absent = NC = corrections direct
PB6	J2/14	I2C_SCL	I ² C	SHT40 (0x44) + TMP102 (0x48), 4.7 k pulls; P5 probe port
PB7	J2/15	I2C_SDA	I ² C	(proto uses AHT10 0x38 <i>alone</i> on the bus — PCB unaffected)

Pin	Hdr	Net	Group	Function / notes
PB10	J1	FAN_TACH	DNP	2-wire fans: tach unused; DNP provision (fan fault inferred from temperature)
PB12–15	J2/1–4	BATLED1–4	GPIO	Battery gauge 25/50/75/100 % (330 Ω each)
PC13	—	on-module LED	GPIO	WeAct module
NRST	J1/5	NRST	Reset	SW1 on-board + P10 external, both → GND

4.2 ArduSimple carrier socket (MOD1) — incl. switchless Pro behavior

UNO-form shield socket, pin map **verified against a physical simpleRTK2B Pro (M3 closed, 2026-07-07)** — silk reads D0=TX1, D1=RX1, D2=RX2, D3–D7 empty, D8=TX2.

Shield pin	F9P signal	Dir (Pro)	Carrier net	Role
D0	TX1 (UART1 TX)	out	GNSS_RX → PA3	NMEA to the watchdog
D1	RX1 (UART1 RX)	in	GNSS_TX ← PA2	Watchdog commands/poll
D2	RX2 (UART2 RX)	in	DOUT_4G	RTCM3 downlink — modem-direct, never through the MCU (silk: <i>XBEE-TX/GPS RX2</i>)
D8	TX2 (UART2 TX)	out	K1.NC + PA10 tap	Modo-B uplink source (silk: <i>XBEE-RX/GPS TX2</i>)
5V	shield power	in	SW_5V	Pro's "5V=OUTPUT" switch OFF
IOREF	logic reference	in	3V3	Defines Pro TX/RX levels
GND ×3	—	—	GND	

All other shield positions (3V3, VIN, RESET, A0–A5, D3–D7, D9–D13, AREF, SDA, SCL): NC per ArduSimple guidance — do not connect unused special pins.

Switchless Pro variants — hardwired UART2 behavior. Pro revisions differ and the difference is operationally critical:

- **Older Pros** carry an *XBEE TO GPS UART* slide switch — it must be **parked on UART1** so the (empty) on-Pro XBee socket does not sit on UART2.
- **Newer Pros have no switch:** the on-Pro XBee socket is *hardwired to UART2*, i.e. permanently in parallel with the carrier's D2/D8 rail pins.

|| **WARNING.** On **both** revisions the Pro's own XBee socket stays **EMPTY** — the modem lives on the carrier's J7/J8. On switchless Pros, **never plug the Pro's "USB XBee" port while the unit is in service:** its FTDI sits directly across UART2 — that is the live RTCM3 corrections downlink. Bench configuration via that port only with the unit out of service.

4.3 XBee socket J7/J8 — including the J8 mirror map

J7 carries module pins 1–10 in order; **J8 pad k = XBee pin $(21 - k)$** — the mirror is easy to get wrong and was previously undocumented outside the copper.

Pad	XBee pin	Net	Role
J7.1	1 VCC	3V3_MODEM	3.3–3.6 V, 2 A peak (U7 rail — not 5 V)
J7.2	2 TX	DOUT_4G	RTCM3 out → F9P RX2 (direct)
J7.3	3 RX	DIN_4G	← K1 COM (uplink in)
J7.4	4 GND	GND	
J7.5	5 RESET	MODEM_RST	SW4G button → GND
J7.6	6 V_USB	USB_VBUS	5 V from J9 enables modem USB (laptop-powered only — no rail backfeed)
J7.7 / J7.8	7 USB+ / 8 USB–	USB_DP/USB_DM	Service USB to J9
J7.9 / J7.10	9 DTR / 10 GND	NC / GND	
J8.1	20 ON/OFF	GND	GND = always ON (floating may never power up)
J8.5 / J8.9	16 RTS / 12 CTS	NC	Flow control disabled
J8.6 / J8.10	15 / 11 GND	GND	
J8.7	14 VREF	3V3_MODEM	Must equal VCC
J8.8	13 LED	MODEM_LED	1.8 V drive → Rmled 1 k + D4G (dim — accepted, audit L4)

4.4 Harness connectors (external interface summary)

Full netlist-derived pin tables: harness-connector-pinout.md.

Conn	Type	Function / key pins
P1	Phoenix 5-pos	GX16-5: 1=24V_IN, 2=GND, 3=IGN_IN (raw 12–24 V)
P2	XH-2	VEH5V in from SD-15B-05
P4	XH-3	Battery: 1=BAT_PLUS, 2=GND, 3=NTC (cell)
P5	XH-4	External I ² C probe (3V3/GND/SDA/SCL)
P6	XH-4	Fan: 5V_FAN/FAN_RET/GND/FAN_TACH_RAW
P8	XH-2	Panel LED (LED_A/LED_K)
P10	XH-2	External reset (NRST/GND)
P11	XH-2	Cutoff: 1=MAIN5V, 2=SYS5V — jumper plug installed when no switch fitted; open P11 = dead board
P12	XH-2	Hotspot NTC probe (NTC_TEMP/GND)
P3 / P13 / H3	—	DNP — harness alternatives superseded by carrier sockets + K1 bypass

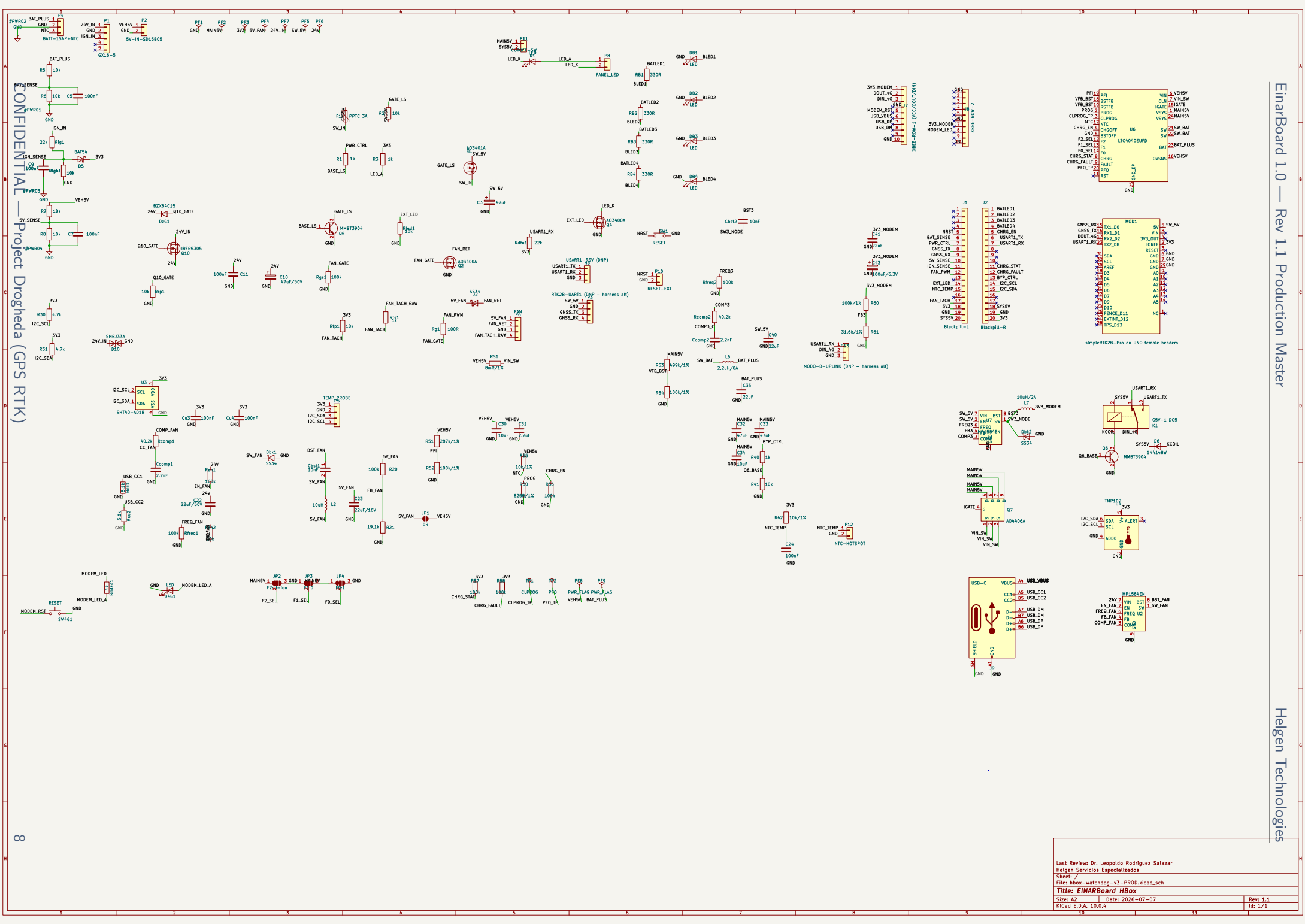
5 PCB fabrication specification

Parameter	Specification
Stackup	4-layer: F.Cu (signal/power) / In1.Cu (solid GND plane) / In2.Cu (signal) / B.Cu
Material	FR-4, standard TG150 (JLCPCB 4-layer default stackup)
Thickness / copper	1.6 mm finished; 1 oz outer copper
Finish	ENIG — required in practice for the QFN-24 (LTC4040), DFN-4 (SHT40), SOT-563 (TMP102) and USB-C fine pitch
Soldermask / silk	Blue mask, white silkscreen (nearest standard to Helgen indigo #2C3C5B); black is the approved alternate — no other colors without brand approval
Min track/space	0.15 mm present on board (JLC 4-layer capability 0.09 mm)
Netclasses	PWR_HI 1.5 mm · PWR_MID 1.0 mm (Rev 1.1/H4 added SW_IN) · default 0.2 mm; exceeds the kicad-guide minimums ($5V \geq 0.5\text{ mm}$, $SW_5V \geq 0.8\text{ mm}$)
Impedance	Not controlled — USB 2.0 FS service port only (audit M5: functional-grade; next spin routes $D\pm$ as a pair + ESD array)
Vias	Tented (default); EP stitching under U6/U2/U7 to In1
Mounting	$4 \times 3.2\text{ mm}$ (MH1-4) at 4–5 mm edge margins — M3 brass standoffs
Order	5 pcs minimum; PCBA = Standard (QFN/fine pitch); SMD by JLC, THT hand-soldered per order guide

Fab exports live in `kicad/production/` (Fabrication Toolkit: Gerbers + BOM.csv + CPL, regenerated *after* the final Rev 1.1 save). The stale `fab-jlc-usb/` package is superseded — do not order from it (audit M6).

6 Schematic — Rev 1.1 full sheet

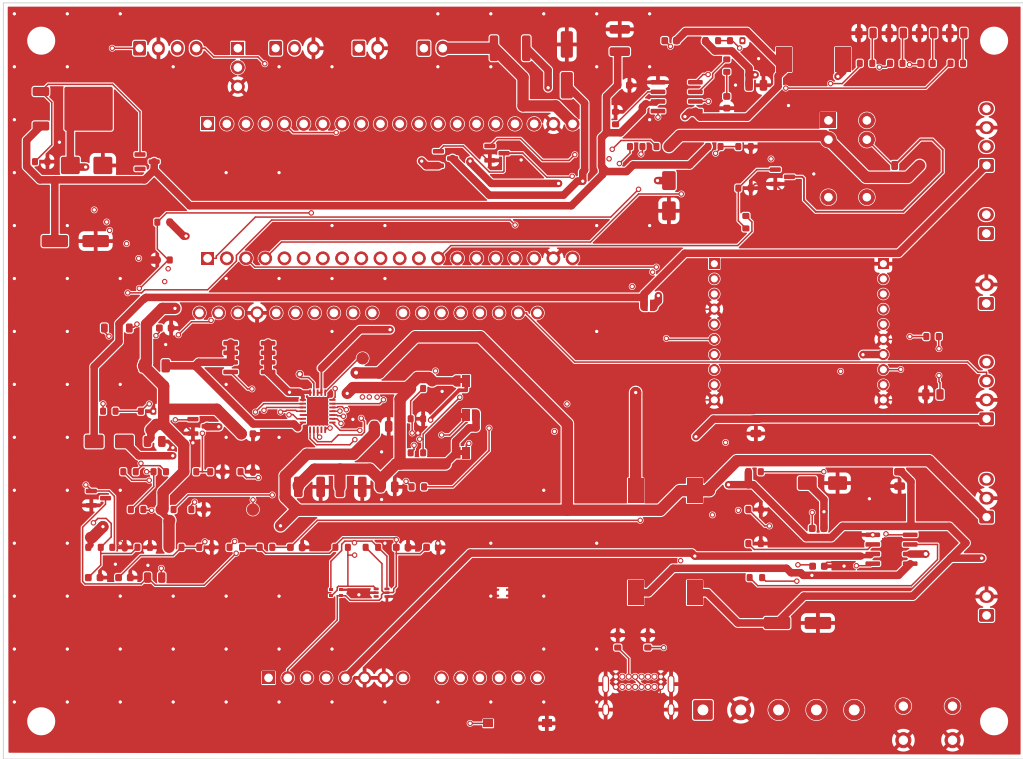
The complete Rev 1.1 production schematic (all blocks A–K + USB service port, post-audit state: Q7 S/D corrected, Q5/Q6 BEC map, RIG1/RDFU1 22 k Ω) is reproduced on the following page, exported from `kicad/hbox-watchdog-v3-PROD.kicad_sch` *after* the 2026-07-07 closure save. The vector original lives at `assets/schematic-rev11.pdf` — zoom there for net-level reading; this page is the archival copy. **Reminder: `sch`↔`board sync` on this project is manual (F8 retired)** — if the schematic changes, the board does not follow automatically.



7 PCB layer plots & assembly view

Per-layer copper plots of the routed board (135.1×100.1 mm, 1317 tracks, 249 vias), each with `Edge.Cuts` overlaid and the KiCad title block, exported from the Rev 1.1 `.kicad_pcb`. All plots are viewed **from the top** (X-ray convention — B.Cu is *not* mirrored). Originals in `assets/layers/`.

Page	Layer	Content
1	F.Cu	Top copper: power routing (PWR_HI 1.5 mm / PWR_MID 1.0 mm incl. SW_IN), module socket fields, LTC4040 block
2	In1.Cu	Solid GND plane (stitched; EP thermal ties for U6/U2/U7)
3	In2.Cu	Inner signal (autoroute overflow; no pour — audit L7)
4	B.Cu	Bottom copper: signal + sense routing
5	F.SilkS	Assembly view: silkscreen + outline, DNP footprints crossed out (P3/P13/H3)



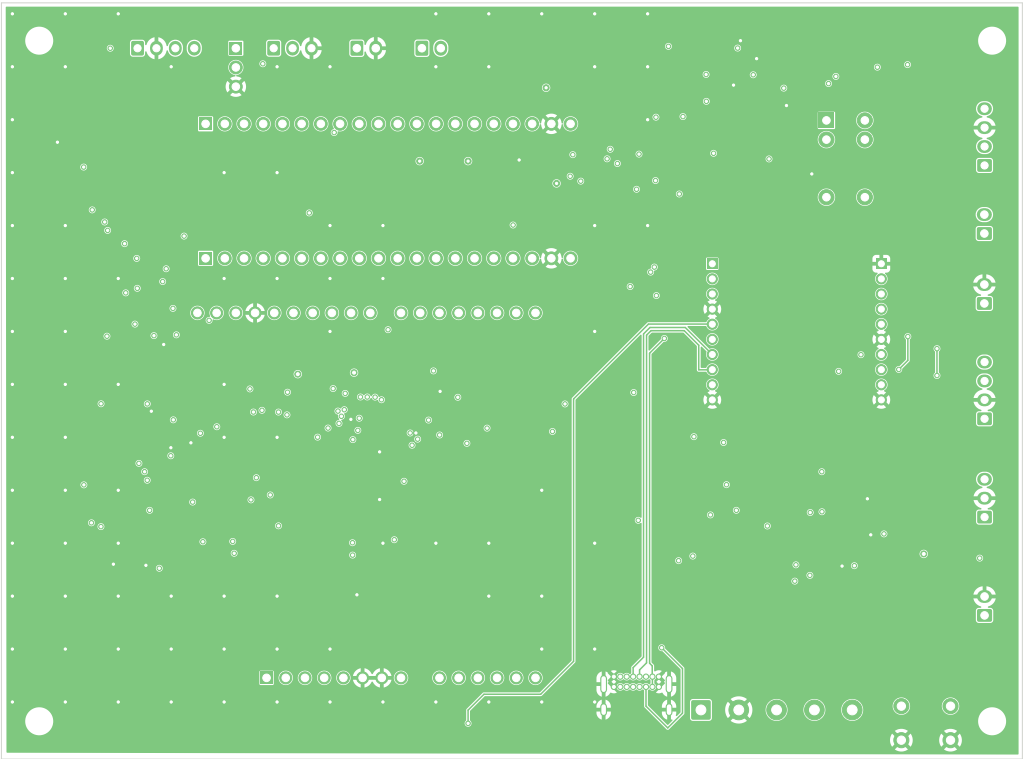
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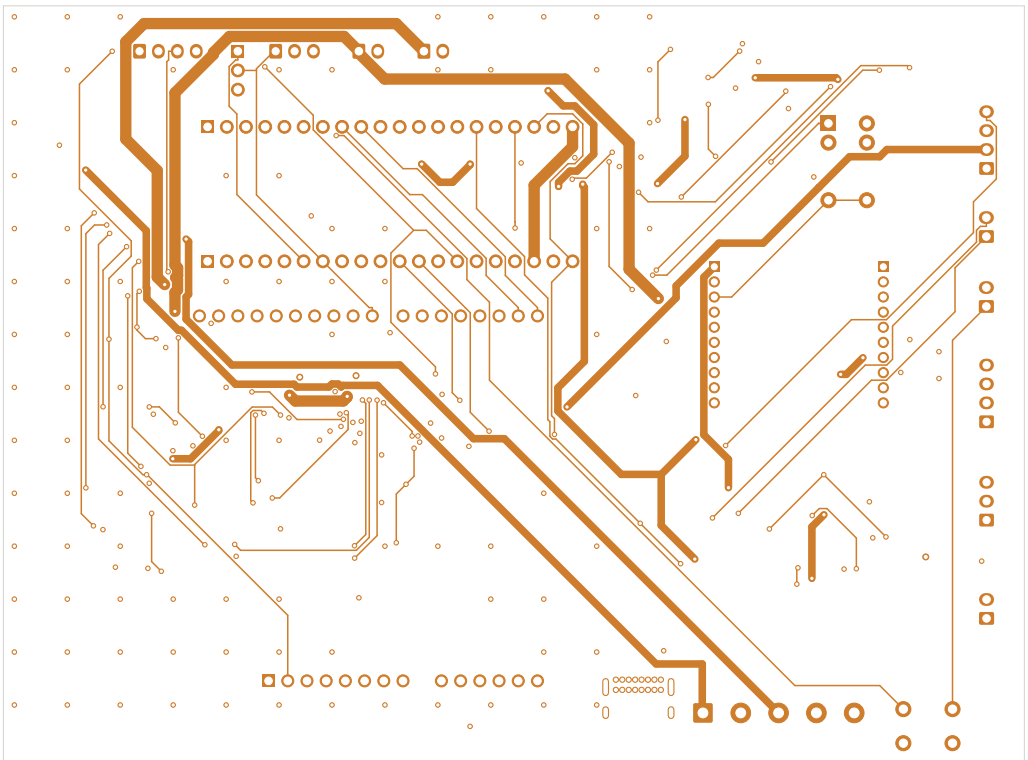
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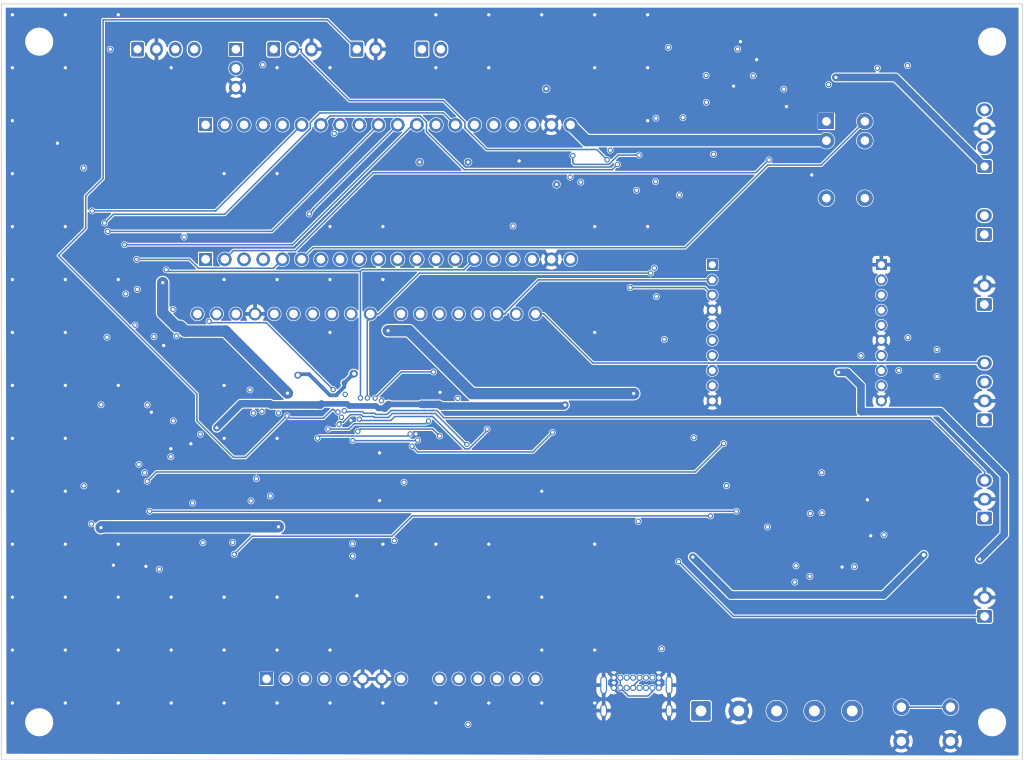
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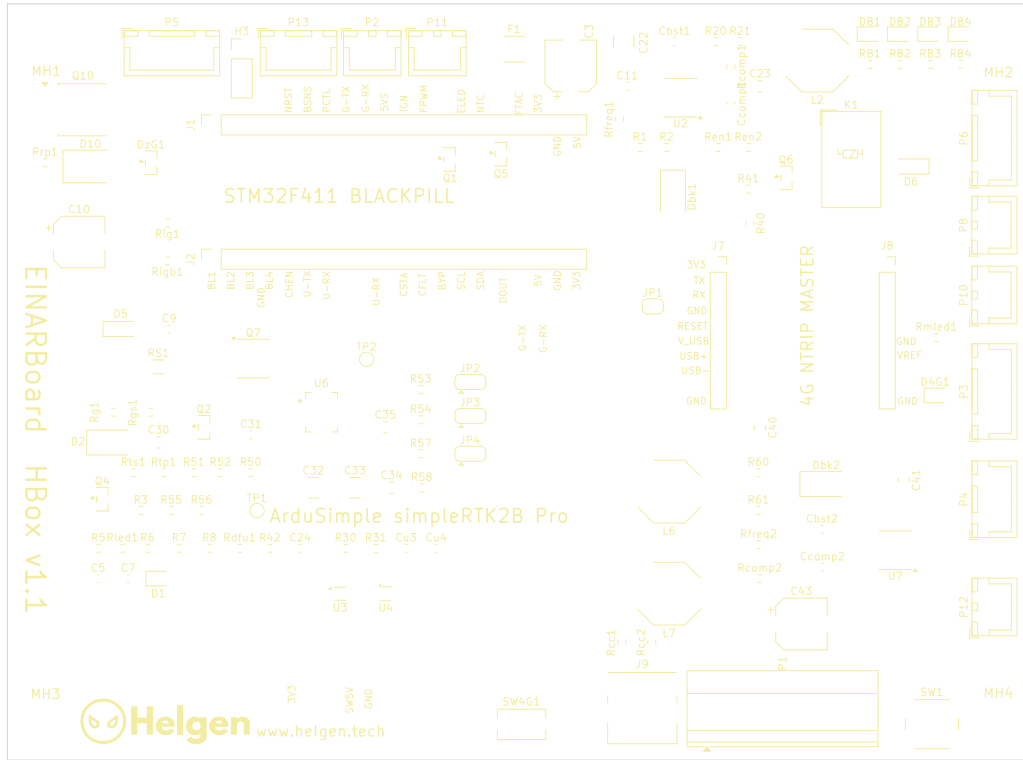
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Title: EINARBoard HBOX 1.1

Size: A4 Date: 2026-06-23
KiCad E.D.A. 10.0.4

Rev: 1.1
Id: 1/1

8 Production BOMs (synchronized)

Both tables below are **generated** — do not edit here. Source of truth: `helgen_einarboard_1.0_production_bom.xls`
regenerate both with `tools/sync_bom.py`.

8.1 Internal PCBA BOM (per board — JLC order)

Table 2: Internal PCBA BOM — per board (synchronized from the production workbook).

Qty	RefDes	Description	Pkg	Part	LCSC	Assy	U
1	U6	Battery-backup manager: 1S Li-ion charger + power-path + 2.5 A boost (Rev 1.1 values: RPROG 825R -> 2.42 A ~ C/5, RS 8 mR -> 3.1 A, F-straps 4.00 V Li-ion)	QFN-24 4x5	Analog Devices LTC4040EUFDF#TRPBF	C687163	SMD (JLC)	
2	U2, U7	Buck 1.5 MHz 3 A — U2: 24 V -> 5V_FAN; U7: SW_5V -> 3V3_MODEM (stack cycle reboots modem)	SOIC-8-EP	MPS MP1584EN-LF-Z	C15051	SMD (JLC)	
1	U3	Relative humidity / temperature sensor, I2C 0x44	DFN-4 1.5x1.5	Sensirion SHT40-AD1B-R3	C2848306	SMD (JLC)	
1	U4	Temperature sensor +/-0.5 degC, I2C 0x48 (ADD0=GND)	SOT-563	Texas Instruments TMP102AIDRLR	C99269	SMD (JLC)	
1	Q7	N-FET 30 V <=13.6 mR — LTC4040 VIN->VSYS disconnect. Rev 1.1 (H1): S=VIN_SW, D=MAIN5V (gate=IGATE)	SOIC-8	AOS AO4406AL	C35349	SMD (JLC)	
1	Q10	P-FET -55 V, 24 V reverse-polarity front end (with DzG 15 V gate zener)	TO-252	Infineon IRFR5305TRPBF	C2624	SMD (JLC)	
1	Q1	P-FET -30 V, RTK-stack high-side load switch (SW_IN -> SW_5V)	SOT-23	AOS AO3401A	C15127	SMD (JLC)	
2	Q2, Q4	N-FET — fan low-side PWM / status-LED driver	SOT-23	AOS AO3400A	C20917	SMD (JLC)	
2	Q5, Q6	NPN drivers — load-switch / K1 coil. Rev 1.1 (H2): Q_NPN_BEC pin map (1=B,2=E,3=C)	SOT-23	onsemi MMBT3904	C20526	SMD (JLC)	
1	K1	Signal relay SPDT 5 V coil — Mode-B fail-safe bypass, NC = F9P TX2 -> 4G DIN (corrections survive dead MCU)	THT DIP	Omron G5V-1 DC5	verify at LCSC	THT (hand)	
1	L6	Power inductor 2.2 uH, Isat 14 A (LTC4040 SW<->BAT)	8.8x8.2 molded	Sunlord MWSA0804S-2R2MT	C17700165	SMD (JLC)	
2	L2, L7	Power inductor 10 uH, Isat 6.5 A (fan buck / modem buck)	8.8x8.2 molded	Sunlord MWSA0804S-100MT	C17700171	SMD (JLC)	
1	RS1	Current-sense resistor 8 mR 1% 1 W (LTC4040 input limit 3.1 A)	1206	FOJAN FRM121WFR008TM	C7420012	SMD (JLC)	
1	F1	PPTC resettable fuse 3 A 24 V (SYS5V -> SW_IN)	1812	LUTE 1812L300/24GR	C20627123	SMD (JLC)	
1	D10	TVS 33 V 600 W, 24 V input clamp	SMB	Littelfuse SMBJ33A	C224019	SMD (JLC)	
1	DzG	Zener 15 V (Q10 gate protection)	SOT-23	onsemi BZX84C15LT1G	C80857	SMD (JLC)	
1	D5	Schottky BAT54 — PA5 ignition clamp to 3V3	SOD-123	BAT54	auto-match	SMD (JLC)	

Qty	RefDes	Description	Pkg	Part	LCSC	Assy	U
1	D6	1N4148W — K1 coil flyback	SOD-123	1N4148W	C2099	SMD (JLC)	
3	D2, Dbk, Dbk2	Schottky 40 V 3 A — fan flyback / buck freewheel x2	SMA	SS34	C8678	SMD (JLC)	
6	D1, D4G, DB1-DB4	LED green 0805 — status, modem, 4-LED battery gauge	0805	—	C28105	SMD (JLC)	
1	R50	825R — LTC4040 PROG: I_CHG = 2000/RPROG = 2.42 A ~ C/5 (12 Ah pack)	0603	—	Basic auto	SMD (JLC)	
1	R51	287k — PFI divider top (VEH5V trip 4.60 V falling)	0603	—	Basic auto	SMD (JLC)	
1	R53	499k — BSTFB/RSTFB divider top (backup 4.79 V; RST -7.5%)	0603	—	Basic auto	SMD (JLC)	
1	R21	19.1k — U2 FB bottom (5V_FAN = 5.0 V)	0603	—	Basic auto	SMD (JLC)	
1	R61	31.6k — U7 FB bottom (3V3_MODEM = 3.33 V)	0603	—	Basic auto	SMD (JLC)	
3	R52, R54, R60	100k 1% — PFI / FB dividers	0603	—	Basic auto	SMD (JLC)	
2	R42, R55	10k 1% — NTC dividers (PB1 hotspot / LTC4040 NTC bias)	0603	—	Basic auto	SMD (JLC)	
2	RIG1, RDFU1	22k — ignition divider top (raw 12-24 V) / DFU pull. Rev 1.1 (H3): corrected from stale 100R	0603	—	Basic auto	SMD (JLC)	
10	R2, R5, R6, R7, R8, R41, Rigb, Rled, Rrp, Rtp	10k — pulls, sense divider halves, Rigb ignition divider bottom	0603	—	Basic auto	SMD (JLC)	
8	R20, R56, R57, R58, Ren1, Rfreq, Rfreq2, Rgs	100k — FB tops, pulls, FREQ set, EN UVLO top	0603	—	Basic auto	SMD (JLC)	
5	R1, R3, R40, Rts, Rmled	1k — base drives, LED limits, tach series	0603	—	Basic auto	SMD (JLC)	
4	RB1-RB4	330R — battery-gauge LED limits (PB12-PB15)	0603	—	Basic auto	SMD (JLC)	
2	R30, R31	4.7k — I2C1 pull-ups (SCL/SDA)	0603	—	Basic auto	SMD (JLC)	
2	Rcomp, Rcomp2	40.2k — MP1584 COMP loop	0603	—	Basic auto	SMD (JLC)	
2	Rcc1, Rcc2	5.1k — USB-C CC1/CC2 device-mode pulldowns	0603	—	Basic auto	SMD (JLC)	
1	Rg	100R — Q2 gate series	0603	—	Basic auto	SMD (JLC)	
1	Ren2	20k — MP1584 EN UVLO bottom (EN abs-max 6 V — never tie EN to 24 V)	0603	—	Basic auto	SMD (JLC)	
7	C5, C7, C9, C11, C24, Cu3, Cu4	100 nF X7R — decoupling, PA5/PB1 filters	0603	—	Basic auto	SMD (JLC)	
2	Cbst, Cbst2	10 nF — MP1584 BST bootstrap (U2/U7)	0603	—	Basic auto	SMD (JLC)	
2	Ccomp, Ccomp2	2.2 nF — MP1584 COMP	0603	—	Basic auto	SMD (JLC)	
1	C31	2.2 uF — U6 VIN aux	0603	—	Basic auto	SMD (JLC)	
2	C30, C34	10 uF X5R — U6 VIN / VSYS	0805	—	Basic auto	SMD (JLC)	
3	C35, C40, C41	22 uF >=16 V — U6 BAT / U7 in / U7 out	0805	—	Basic auto	SMD (JLC)	

Qty	RefDes	Description	Pkg	Part	LCSC	Assy	U
1	C23	22 uF 16 V — U2 buck out	0805	—	Basic auto	SMD (JLC)	
1	C22	22 uF 50 V — U2 buck in (24 V node)	1210	—	Basic auto	SMD (JLC)	
2	C32, C33	47 uF >=25 V low-ESR ceramic — VSYS hold-up (with C34: 104 uF >= datasheet 100 uF min)	1210	—	Basic auto	SMD (JLC)	
1	C3	47 uF radial electrolytic — SW_5V bulk	radial 5x7	—	auto/hand	THT (hand)	
1	C10	47 uF 50 V radial — 24 V bulk	radial 6.3x7.7	—	auto/hand	THT (hand)	
1	C43	100 uF 6.3 V radial — 3V3_MODEM bulk (LTE TX bursts)	radial 6.3x7.7	—	auto/hand	THT (hand)	
1	J9	USB-C receptacle USB 2.0 (modem service console: VBUS->J7.6 enables modem USB; no rail backfeed)	SMD 14P	GCT USB4085-GF-A	search USB4085	THT/SMD (hand rec.)	
1	SW4G	Tactile switch SMD — modem RESET (J7.5 -> GND)	6x3.5 gull-wing	C&K PTS636SK25SMTRLFS	C2689642	SMD (JLC)	
1	SW1	Tactile 6 mm THT — MCU RESET (NRST -> GND)	THT 6 mm	—	hand	THT (hand)	
1	P1	Terminal block 5-pos 5.08 mm — GX16 machine power in (24V_IN / GND / IGN_IN)	THT	Phoenix MKDS 1,5/5-5,08	hand	THT (hand)	
5	P2, P8, P10, P11, P12	JST-XH 2-pin top-entry — 5V-IN, panel LED, ext reset, cutoff switch, hotspot NTC	THT B2B-XH	JST B2B-XH-A	hand	THT (hand)	
1	P4	JST-XH 3-pin — battery 1S4P: BAT+ / GND / NTC	THT B3B-XH	JST B3B-XH-A	hand	THT (hand)	
2	P5, P6	JST-XH 4-pin — I2C probe port / fan (5V_FAN, RET, GND, TACH)	THT B4B-XH	JST B4B-XH-A	hand	THT (hand)	
2	J1, J2	Female header 1x20 2.54 mm — Blackpill socket	THT	—	hand	THT (hand)	
2	J7, J8	Female socket 1x10 2.00 mm — XBee 4G socket (rows 22.35 mm)	THT	—	hand	THT (hand)	
1	MOD1	Arduino-UNO female header kit 10+8+8+6 — simpleRTK2B Pro shield socket	THT 2.54	—	hand	THT (hand)	
0	P3, P13, H3	DNP — harness alternatives made redundant by carrier sockets + K1 NC bypass (P3 UART1 tap, P13 Modo-B uplink, H3 USART1 header)	THT	—	—	DNP	
0	JP1	0R rail-select option — OPEN by default (dedicated fan buck); close ONLY if SD-15B-05 upsized	0603	—	C21189	DNP	
TOTAL — PCBA parts per h							

8.2 External Integration BOM (per HBOX unit — Helgen procurement)

Everything the unit needs *around* the PCBA: enclosure set (HBOX-135100), the three plug-in modules, antennas, the 1S4P pack, cabinet-side power and panel hardware, and the pre-wired JST harnesses. Order these in parallel with the boards — module lead times (ArduSimple) usually pace the build, not the PCB.

Table 3: External Integration BOM — per HBOX unit (enclosure, modules, pack, panel, harnesses; NOT in the JLC order).

Qty	Part	Description / notes	Source / MPN	Unit \$	Line \$
1	HBOX-135100 enclosure set	ASA printed base + top + brackets, resized for the 135x100 mm carrier (IP67 strategy: conduction, no vents) — <i>Mechanical fit VERIFIED 2026-07-07 (audit M4 closed)</i> .	Helgen in-house (SKU HBOX-135100)	18.00	18.00
4	M3 brass standoff M3x10	Board mount — MH1-MH4, 3.2 mm holes — 4-5 mm edge margins per audit.	generic brass	0.15	0.60
8	M3x6 screw, zinc	Standoff top + enclosure boss	generic	0.03	0.24
1	Thermal interface pad set	Conduction path: pack/modem hotspot -> enclosure wall — <i>Supports canonical invariant #4</i> .	generic silicone 1.5 mm	1.20	1.20
1	simpleRTK2B Pro (ZED-F9P)	GNSS RTK receiver, seats into MOD1 as UNO shield — <i>Switch/switchless revisions — see manual field warnings</i> .	ArduSimple AS-RTK2B-PROF9P-L1L2-NH-00	210.00	210.00
1	4G NTRIP Master (XBee LTE)	Corrections modem, seats into J7/J8 (3V3_MODEM) — 2 A peak at 3.3 V (audit L5).	ArduSimple AS-XBEE-4G-NA-UFL-00	155.00	155.00
1	STM32F411 Blackpill (WeAct)	Watchdog MCU, seats into J1/J2 — <i>Flash via USB-C DFU (H1 SWD dropped)</i> .	WeAct STM32F411CEU6	6.50	6.50
1	u-blox multiband GNSS antenna	L1/L2 survey antenna, SMA	ArduSimple AS-ANT2B-ANN-L1L2-50SMA	65.00	65.00
2	LTE antenna	4G blade antenna, u.FL/SMA per modem kit	AR1582	8.00	16.00
4	18650 Li-ion cell ~3 Ah	1S4P pack, 3.6 V nominal — charge 4.00 V strap (cycle life + hot-cell margin, RCA #1) — <i>Pack ~12 Ah confirmed 2026-06-30</i> .	quality tier-1 cell (e.g. INR18650)	4.50	18.00
1	1S4P pack hardware	Holder / nickel strip / lead set + heatshrink	generic	3.00	3.00
1	Pack NTC 10k B3950	Bonded to cell, wired to P4.3 (charger-owned NTC) — <i>B3380 ideal; B3950 accepted (trip shifts a few degC — bring-up note)</i> .	generic epoxy bead	0.30	0.30
1	Mean Well SD-15B-05	24->5 V 3 A supply feeding VEH5V (P2) — <i>RS1 3.1 A input limit protects this unit</i> .	Mean Well SD-15B-05	14.50	14.50
1	GX16-5 connector pair	Panel + cable plug: 1=24V_IN, 2=GND, 3=IGN_IN (RAW 12-24 V) — <i>Pin 3 carries RAW ignition — Rev 1.1 divider (22k/10k) expects it</i> .	GX16-5	2.20	2.20
1	Panel-mount dual LED	External status indicator, wired to P8 (LED_A/LED_K)	generic 8 mm dual-color	0.80	0.80
1	Cutoff switch SPST panel	P11 in series MAIN5V->SYS5V — kills vehicle AND battery — <i>Ship P11 with jumper plug installed — open P11 = dead board</i> .	generic 21x15 rocker/toggle	1.50	1.50
1	External reset button	Panel momentary NO, wired to P10 (NRST/GND)	generic 12 mm	0.60	0.60
1	Fan 5 V 2-wire	Ducted per thermal v3.0 concept; PWM low-side — <i>2-wire: no tach — fan fault inferred from temperature</i> .	generic 40x40 5 V	3.50	3.50
1	External NTC probe 10k B3950	Cabinet hot-spot probe, wired to P12	generic sealed probe	0.50	0.50
5	JST-XH 2-pin pre-wired harness	P2 5V-IN / P8 panel LED / P10 reset / P11 cutoff / P12 NTC — 22-24 AWG, 300 mm — <i>Power pairs (P2/P11) in 22 AWG</i> .	JST XHP-2 + pre-crimped	0.35	1.75
1	JST-XH 3-pin pre-wired harness	P4 battery: BAT+ / GND / NTC — 20 AWG power pair	JST XHP-3 + pre-crimped	0.40	0.40
2	JST-XH 4-pin pre-wired harness	P5 I2C probe / P6 fan	JST XHP-4 + pre-crimped	0.45	0.90
1	JST-PH pre-wired set (spares)	PH 2.0 mm pigtails for space-constrained sensor drops — <i>Optional — XH is the board standard</i> .	JST PHR-2/3	0.40	0.40

continues

Qty	Part	Description / notes	Source / MPN	Unit \$	Line \$
1	Telcel M2M micro-SIM	LTE data for NTRIP corrections — <i>Cost = monthly plan, not BOM.</i>	Telcel M2M plan	0.00	0.00
TOTAL — external integration per unit					520.89

9 Assembly & field warnings

1. **Switchless simpleRTK2B Pro variants** — see §4.2: XBee socket empty on both revisions; switch (if present) parked on UART1; **never** the Pro's USB-XBee port in service.
2. **P11 cutoff** ships with a jumper plug when no panel switch is fitted — an open P11 is a dead unit that looks like a field failure.
3. **GX16 pin 3 = raw ignition.** Harnesses must feed 12–24 V machine ignition, *not* a pre-conditioned 5 V (the DFR1015 stage no longer exists).
4. **Battery pack:** 1S4P only, cell NTC bonded and wired to P4.3 — the charger owns that NTC. Verify the 4.00 V strap set (JP2/3/4) before connecting a pack.
5. **Modules are hand-fitted** after PCBA; they are never on the JLC BOM. Seat the Pro with the notch/silk alignment — D0/D1 reversal is fatal to the GNSS UART and invisible electrically.
6. **IP67 discipline:** conduction cooling only; thermal pads from pack/modem hotspot to the enclosure wall; no vents.
7. **CPL rotation spot-check** at JLC review: LTC4040 (QFN-24) and both MP1584 (SOIC-8-EP) orientations, plus Q7 — rotation errors are the #1 PCBA failure and H1 taught us what a reversed Q7 costs.

10 Order readiness & open gates

- **CLEARED:** H1–H4 fixed and re-verified (ERC 0 / DRC 0); M3 closed on a physical Pro; M4 (HBOX mechanical fit) verified 2026-07-07; fab package regenerated after the last save. **Bare-board order: RELEASED.**
- **OPEN — M1 remainder (PCBA):** specialty + semiconductor LCSC numbers are verified and baked into the schematic (18 pinned lines); passives ride JLC auto-match at upload; DNP attributes on P3/P13/H3 confirmed in Rev 1.1. Re-confirm live stock at upload — the pacing item is parts, not fab.
- **OPEN — M2 (deliberate risk posture):** the declared fab gate — *bench-validate the LTC4040 backup transition + hot-cell charge cutoff* — remains unmet by the TP4056 proto. Bare boards at 5 pcs are the cheap, conscious way to retire it; **do not commit the 30-unit PCBA run before the LTC4040 block passes on real copper.**
- **Known-accepted:** USB service port is functional-grade (M5); D4G dim at 1.8 V drive (L4); L7 saturation margin thin vs 2 A modem peak (L5) — 3 A part next spin.

Appendix — BOM synchronization toolchain

Single source of truth = the Excel workbook. Flow:

1. `python3 tools/generate_production_bom.py` — (re)builds `helgen_einarboard_1.0_production_bom.xls` (Summary + Internal PCBA + External Integration, Helgen palette, live line-cost and cross-sheet roll-up formulas).
2. Edit costs/parts in Excel as quotes land (or edit the generator and re-run).
3. `python3 tools/sync_bom.py` — extracts the *Internal PCBA BOM* and *External Integration BOM* tabs, drops section bars / blanks / TOTAL rows, escapes LaTeX reserved tokens (&, _, %, \$, #, {}, ~, ^, \), recomputes line costs, writes `pcba_bom.tex` + `external_bom.tex`.
4. `pdflatex einarboard-manual.tex` ×2 — the manual ingests both snippets via `\input{}`.

Drawing assets (`assets/`): `schematic-rev11.pdf` (full A2 sheet) + `layers/` (per-layer plots) + `board-assembly-top.pdf` are exported from the Rev 1.1 KiCad files via `kicad-cli` (KiCad MCP) —

re-export after *any* board/schematic save, or the manual silently archives stale copper. The Jun-22 watchdog-pcb-v3-blockdiagram.svg predates the carrier conversion and is deliberately *not* included. KiCad board ↔ schematic sync on this project is **manual** (F8 retired after the refdes-duplication incident) — never let a BOM edit imply a netlist push.

Helgen Technologies — precise, fail-safe first.

Canonical electrical state: watchdog-electrical-design-state.md · Audit:

2026-07-06_Drogheda_EinarBoard-1.0-PreFab-Audit_v1.0.md